Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) A method for sharing a general purpose input/output (GPIO) line of an integrated circuit between at least two circuit components, the method comprising:

providing, using the GPIO line, a first input from a first circuit component to the integrated circuit during a first time;

providing, using the GPIO line, a first output from the integrated circuit to a second circuit component during a second time; and

wherein the first circuit component and the second circuit component are concurrently coupled to the GPIO line.

2. (original) The method of Claim 1, wherein the step of providing the first input includes providing the first input at a low frequency relative to a switching frequency of the GPIO line.

3. (original) The method of Claim 2, wherein the first time is at least in part concurrent with the second time.

4. (original) The method of Claim 1, wherein the first time is different from the second time.

5. (original) The method of Claim 1, further comprising the step of providing, using the GPIO line, a second input from the first circuit component to the integrated circuit during a third time different from the first time.

6. (original) The method of Claim 1, further comprising the step of providing, using the GPIO line, a second output from the integrated circuit to the second circuit component during a third time different from the second time.

7. (original) The method of Claim 1, wherein the step of providing a first input comprises the step of configuring the GPIO line as an input line during a portion of the first time, and the step of providing a first output comprises the step of configuring the GPIO line as an output line during the second time.

8. (currently amended) The method of Claim 7, wherein:

the portion of the first time includes a first predetermined sequence of processing cycles; and

the second time includes a second predetermined sequence of processing cycles different from the first sequence.

9. (original) The method of Claim 1 , wherein the first circuit component includes a switch.

10. (original) The method of Claim 1, wherein the second circuit component includes a light emitting diode.

11. (original) The method of Claim 10, wherein the second circuit component further includes an inverter.

12. (original) The method of Claim 1, wherein the integrated circuit comprises one or more of a group consisting of: a microprocessor, a microcontroller, a field programmable gate array, a programmable logic device, a programmable logic array, and an application specific integrated circuit.

13. (original) A method for sharing a general purpose input/output (GPIO) line of an integrated circuit, the method comprising:

connecting a first component to the GPIO line

connecting a second circuit component to the GPIO line concurrently with the first circuit component;

wherein the first circuit component is to provide input to the integrated circuit using the GPIO line during a first time; and

wherein the second circuit component is to receive an output from the integrated circuit using the GPIO line during a second time.

14. (original) The method of Claim 13, wherein the step of providing the first input includes providing the first input at a low frequency relative to a switching frequency of the GPIO line.

15. (original) The method of Claim 14, wherein the first time is at least in part concurrent with the second time.

16. (original) The method of Claim 13, wherein the first time is different from the second time.

17. (original) The method of Claim 13, further comprising the steps of:

configuring the GPIO line as an input line during a portion of the first time; and

configuring the GPIO line as an output line during the second time period.

18. (currently amended) The method of Claim 17, wherein:

the portion of the first time includes a first predetermined sequence of processing cycles; and

the second time includes a second predetermined sequence of processing cycles different from the first sequence.

19. (original) The method of Claim 13, wherein the first circuit component includes a switch.

20. (original) The method of Claim 13, wherein the second circuit component includes a light emitting diode.

21. (original) The method of Claim 20, wherein the second circuit component further includes an inverter.

22. (original) The method of Claim 13, wherein the integrated circuit is one of a group consisting of: a microprocessor, a microcontroller, a field programmable gate array, a programmable logic device, a programmable logic array, and an application specific integrated circuit.

23. (original) An electrical circuit having circuit components in electrical communication with an integrated circuit, the circuit being adapted to share a general purpose input/output (GPIO) line of the integrated circuit among at least two circuit components external to the integrated circuit, the circuit comprising:

a first circuit component connected to the GPIO line;

a second circuit component connected to the GPIO line concurrently with the first circuit component;

the integrated circuit being adapted to receive an input from the first circuit component via the GPIO line during a first time; and

the integrated circuit being adapted to provide an output to the second circuit component via the GPIO line during a second time.

24. (original) The circuit of Claim 23, wherein the first circuit is adapted to provide the first input at a low frequency relative to a switching frequency of the GPIO line.

25. (original) The circuit of Claim 24, wherein the first time is at least in part concurrent with the second time.

26. (original) The circuit of Claim 23, wherein the first time is different from the second time.

27. (original) The circuit of Claim 23, wherein the GPIO line is configured as an input line during a portion of the first time, and the GPIO line is configured as an output line during the second time.

28. (currently amended) The circuit of Claim 27, wherein the portion of the first time includes a first predetermined sequence of processing cycles, and the second time includes a second predetermined sequence of processing cycles different from the first sequence.

29. (original) The circuit of Claim 23, wherein the first circuit component includes a switch.

30. (original) The circuit of Claim 23, wherein the second circuit component includes a light emitting diode.

31. (original) The circuit of Claim 30, wherein the second circuit component further includes an inverter.

32. (original) The circuit of Claim 23, wherein the integrated circuit comprises at least one of a group consisting of: a microprocessor, a microcontroller, a field programmable gate array, a programmable logic device, a programmable logic array, and an application specific integrated circuit.

33. (original) In a system comprising electrical circuitry and components:

an integrated circuit having a general purpose input/output (GPIO) line;

a first circuit component coupled to the GPIO line, wherein the first circuit component is adapted to provide, at a first time, a first input to the integrated circuit using the GPIO line; and

a second circuit component coupled to the GPIO line, wherein the second circuit component is adapted to receive, at a second time, a first output from the integrated circuit using the GPIO line.

34. (original) The system of Claim 33, wherein the first circuit component further is adapted to provide the first input at a low frequency relative to a switching frequency of the GPIO line.

35. (original) The system of Claim 34, wherein the first time is concurrent with the second time.

36. (original) The system of Claim 33, wherein the first time is different from the second time.

37. (currently amended) The system of Claim 36, wherein:

the first time includes a first predetermined sequence of processing cycles; and

the second time includes a second predetermined sequence of processing cycles different from the first sequence.

38. (original) The system of Claim 33, wherein the integrated circuit comprises at least one of a group consisting of: a microprocessor, a microcontroller, a field programmable gate array, a programmable logic device, a programmable logic array, and an application specific integrated circuit.

39. (original) The system of Claim 33, wherein the first circuit component includes a switch.

40. (original) The system of Claim 33, wherein the second circuit component includes a light emitting diode.

41. (original) The system of Claim 40, wherein the second circuit component further includes an inverter.

42. (original) The system of Claim 33, wherein the system comprises a communications modem.

43. (original) The system of Claim 42, wherein the communications modem includes the first and second circuit components.

44. (original) The system of Claim 43, wherein the system is a DSL communications system.